A Low Voltage, Low Power P-Channel EEPROM Cell for Embedded and System-On-A-Chip Applications

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Abstract

A single poly p-channel EEPROM cell is described. The cell, which uses 85A tunnel oxide, employs a novel voltage division scheme to reduce the absolute program and erase voltages to less than 7.5V. This low cost, low power technology is ideally suited for easy integration into deep sub-0.5um, low voltage, logic processes for embedded, portable and system-on-a-chip applications.

Introduction

Many emerging applications, from smart cards to system-on-a-chip require low voltage and/or low power operation with on board non-volatile memory. Single poly, n-channel EEPROM cell technologies have been previously reported [1]. However, these typically require high program/erase voltages of about 12V to operate (i.e., on chip voltages >≅ 14-16V).

In this paper, we describe a small area (31um^2 with 0.5µm design rules), high endurance, p-channel EEPROM cell[2]. This cell, which employs a novel voltage division scheme to reduce the maximum on chip voltage, requires program/erase voltages of less than +7.5V/-7V. The cell is programmed by a combination of band to band tunneling (BTBT)[3] and Fowler-Nordheim tunneling (FN) of electrons. Programming current is <≅ 10nA/cell due to the high programming efficiency. Erase is achieved with low current FN tunneling (<<1nA).

A flash version of this cell will have an area of 17µm2, < 8µm2 and < 6µm2 at 0.5µm, 0.35µm and 0.25µm design rules, respectively. The large area reduction is achieved with the elimination of the erase gate in Fig. 2. Sector erase will be by FN tunneling through read transistor channel oxide.

Cell Structure and Operation

Fig.1 shows the cell circuit schematic. Both the control and the erase gates are in separate triple wells (N+/PW/NW/p-sub). By allowing the PW to float, this structure enables the application of both positive and negative voltages to the N+ nodes. Figure 2 is a schematic cross section of the CG, EG and the read transistor. The cell bias conditions during program, erase & read are shown in Table 1.

Table 1 Cell Bias Conditions

	Vd	Vsg	Vcg	Veg	Vs	Vnw
Prog.	-7	-9	7.5	Float	Float	0
Erase	Float	8.5	-7	7	Float	0
Read	0.7	0.5	Vcc	Float	Vcc	Vcc

To program the cell to the ON state, electrons generated at the read transistor drain by BTBT/FN (Vd= -7V, Vcg= 7.5V, Vnw= 0V) are injected through the read transistor's 85Å gate oxide into the poly floating gate. The cell is erased at the erase gate by FN tunneling of electrons from the floating gate through the 85Å tunnel oxide (Vcg= -7V, Veg= 7V).

Cell Characteristics

The characteristics of the triple well structure for the erase and control gates are shown in Fig. 3(a) and Fig. 3(b) for negative and positive bias on the N+ gate electrodes, respectively. The EG and CG nodes can support low leakage and high breakdown for +7.5V/-7V operation during write.

Fig. 4 shows the programming characteristics of the EEPROM cell for tunnel oxides of 85Å and 90Å (as grown on p-substrate). The control gate coupling for this cell was 70%. High speed programming to Vt>~ 2V is achieved in 400µs. As shown in Fig. 5, this would correspond to very satisfactory read currents of 35µA and 25µA at Vcc= 3V & 2.4V, respectively. For low Vcc operation below 2V, the read current can be increased, if necessary, by adjusting the select transistor width (Tox= 180Å). The high injection efficiency of BTBT/FN programming at 90C is shown in Fig. 6, where the high gate/drain current ratio, Ig/Id, of around 0.3% is illustrated at Vfg= 3.5V and Vd= -7V.

Fig. 6 indicates that under nominal erase conditions of Veg= 7V and Vcg= -7V, the cell can be erased to an OFF state (Vt <= -0.5V) in about 200µs for an upper tunnel oxide thickness limit of 90Å.

Fig. 8 illustrates the cell endurance characteristics at up to 100K cycles. Based on limited samples using a 64Kb product, we have successfully demonstrated high endurance cycling greater than 300K cycles with this technology. These results will be reported in a future publication. Typical data retention characteristics at 250C on fresh cells and cells cycled up to 100K cycles are shown in Table 2. Little charge loss is observed after up to 170 hours of bake. Again, limited data on 64Kb product tend to support the single cell results. These will also be published after more complete data are available.

Conclusions

A small, low cost, low voltage, low power, p-channel EEPROM cell has been demonstrated. With only one extra implant mask compared to the n-channel, single poly EEPROM cell process, we believe this is a very attractive solution for low Vcc applications requiring less than 1Mb of non-volatile memory.

References

1. R. Barsan *et al.,* Non-Volatile Semiconductor Memory Workshop Tech. Dig., paper 1.1, 1995.
2. Ted Chang, Prog. Microelectronics Corp., US Pending Patents No. 08/744699 & 08/560259
3. T. Ohnakado et al., IEDM Tech. Dig., pp. 279-282, 1995.

	Vth (V)			
	Initial	24 hour bake	48 hour bake	170 hour bake
Fresh Cell	3.00	2.73	2.71	2.67
After 10K Cycles	3.00	2.78	2.76	2.72

Table 2: Data Retention Characteristics at 250C

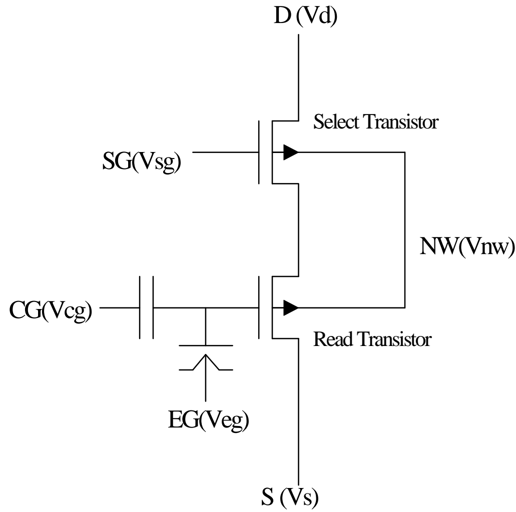
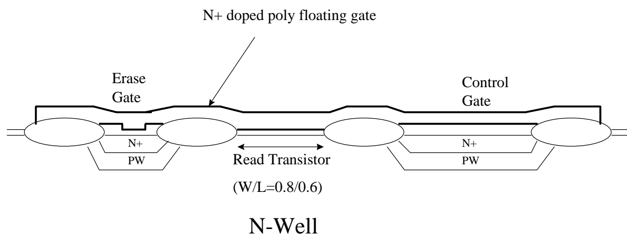


Fig.1 EEPROM cell schematic. The N+ CG and EG nodes are in separate triple wells.



P-Sub

Fig. 2 Cell schematic cross-section

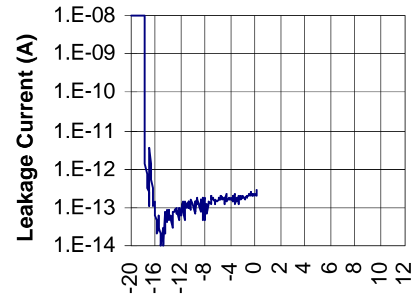


Fig. (3a) Negative N+ bias

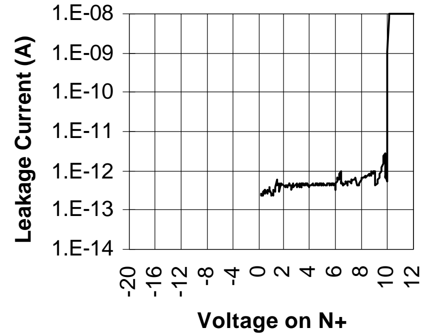


Fig. (3b) Positive N+ bias

Fig.3 Erase & control gate triple well characteristics (T= 25C)

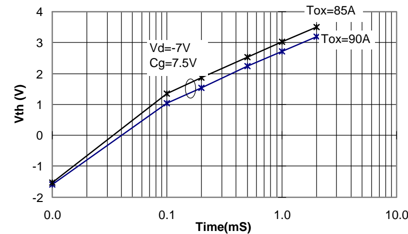


Fig.4 Cell program Vt vs. Programming time for tunnel oxide Tox=85A and 90A

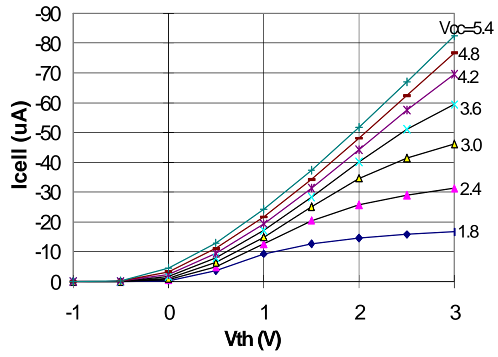


Fig.5 Cell read current vs. Vt for different Vcc (tunnel oxide Tox= 90A, select transistor Tox= 180A, select transistor W/L=1.2/0.8, read transistor W/L=0.8/0.6)

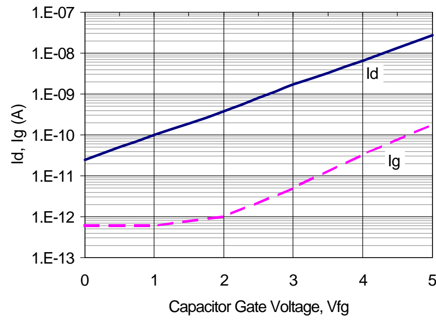


Fig.6 Cell capacitor BTBT/FN Id, Ig vs. Vfg (Vd=-7V, T=90C Tox= 85A)

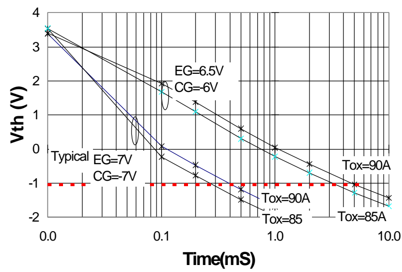


Fig.7 Cell erase Vt vs. Erase time under different erase bias conditions for tunnel oxide Tox= 85A & 90A

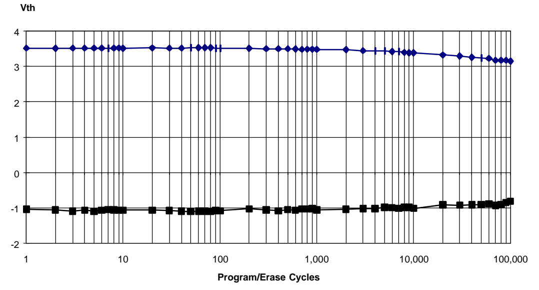


Fig. 8 Cell endurance characteristics (Tox= 90A)