

An Innovative NVM Technology for Sub-0.25um SOC Applications

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Contents

- Market demands & application requirements
- Challenges in embedding flash
- Design for an ideal embedded flash technology
- PMC's approach and solutions
- Technology highlights
- Comparison with other technologies
- PMC status update
- Summary

System-On-Chip (SOC) Requirements

Key Blocks

MCU/DSP core

App. Spec. Logic

PLL, Timers

A/D, Bus arch.

Emb. SRAM

Emb. DRAM

Emb. ROM

Emb. Flash/E²

Functions

Processor

Logic design

Timing control

I/O interface

Cache memory

Data storage (DS)

Prog. code (OS)

ISP code/NV DS

Process Tech.

CMOS logic

CMOS logic

CMOS, M/S

CMOS, M/S

CMOS logic/SRAM

CMOS DRAM

CMOS ROM

CMOS **NVM (HV)**

- Only Embedded Flash/E² provides **Non-volatile In-System Programmability** (ISP) program code and/or data storage -- for high-security **adaptive intelligence** and **(remote) upgrade-ability** against **product obsolescence**
- Only Embedded E² provides on-chip electrical redundancy/repair capabilities for SOC applications where **configurable built-in self correction/repairing** is a must.
- The **challenges** for Embedded Flash/E² are **high voltage reduction, CMOS logic process compatibility** and **scalability**

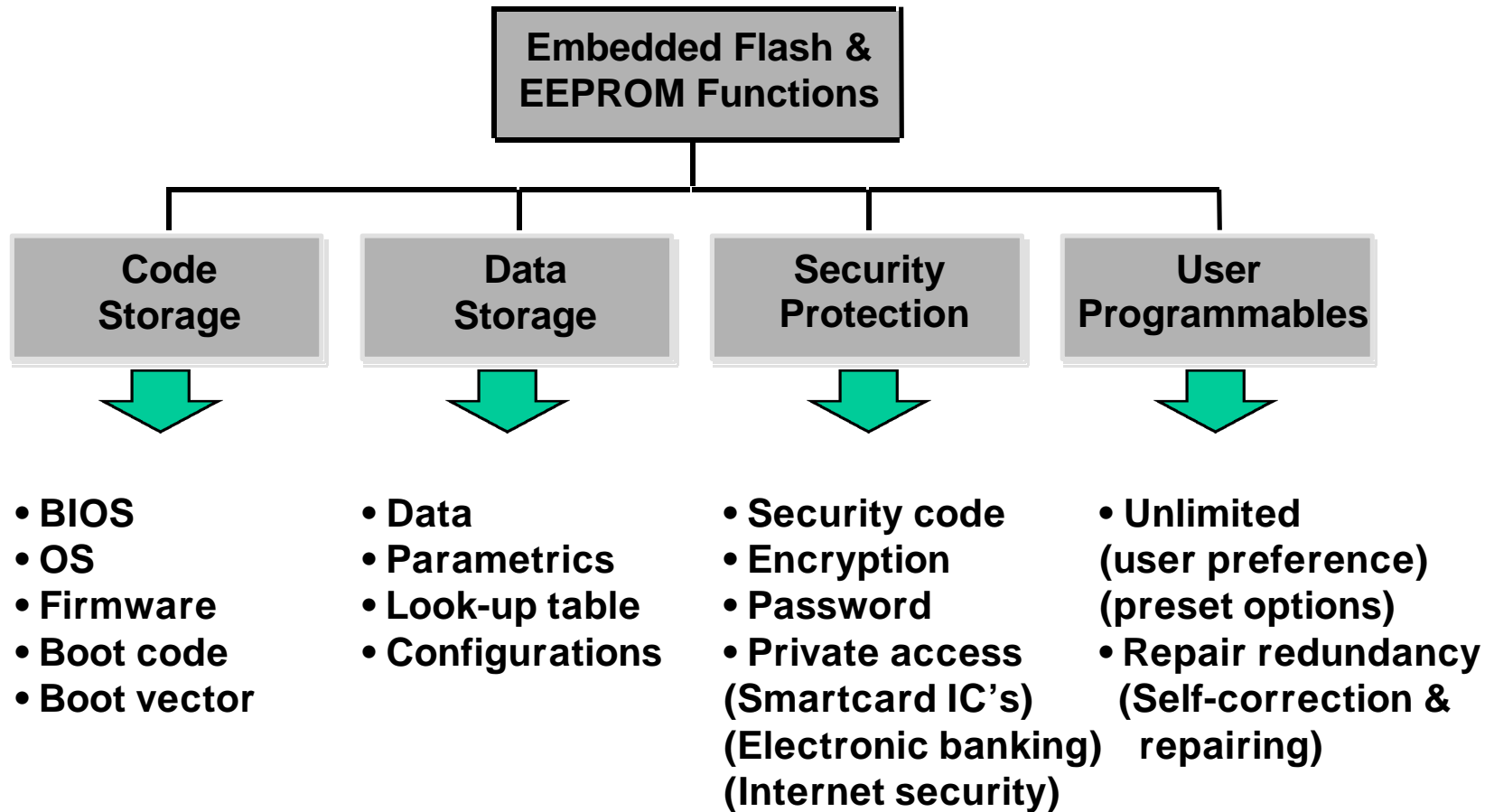
Embedded ISP NVM Market Outlook

- **Semico forecasted Embedded Flash being “a sleeping giant”:**
 - From \$836M in 1997 to \$4.9B by 2001
 - **In-System Programmability (ISP) for high-end MCU’s:**
 - **Over \$10 billion** of annual MCU sales since 1995
 - On-chip Flash has higher values (as compared to ROM):
 - \$41 for uPD70F3008Y vs. \$17 for uPD703008Y
 - \$48.5 for 68HC916Y3 vs. \$25.95 for 68HC16Y3
 - **Smartcard IC’s** incorporating Embedded EEPROM:
 - Market leaders all have Embedded EEPROM features
 - Embedded **Flash/E²PROM** for **RISC, DSP, too.**
 - **“System-on-Chip”** needs **Embedded Flash/EEPROM:**
 - ISP NVM is a must for 0.25um and beyond
 - Prefer both emb. Flash & EEPROM on-chip for ease-of-use
 - Applications are pervasive & virtually unlimited
 - PMC has been recognized for its **sub-0.3um Embedded ISP NVM solutions w/ distinct, comprehensive and solid patent portfolio**
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Foundry Technology Trend

- **Logic products/processes are preferred:**
 - The TAM for logic products is bigger than memories
 - More new applications/customers, higher growth potentials
 - Logic products have higher GPM's than memories
- **Logic process trend is to embedded applications:**
 - On-chip memories are imperative for high-end applications
 - Embedded DRAM is available now for higher integration
 - SOC capability w/ ISP is a must for 0.25um and beyond
 - Embedded Flash/E² is imminent and will be a winning factor
- **Key issues on Embedded Flash/E²:**
 - Too few solutions for sub-0.3um CMOS logic base-line
 - Need multi-generation manufacturable and scalable solution
 - Comprehensive IP coverage to avoid legal problems is a must!!

Functions of Embedded ISP NVM



Flash is good for **mass** code and data storage with **less frequent updating**;
EEPROM, for **smaller-segment** code and data storage **with routine updating**.
For cost-effective SOC applications, **both embedded Flash & EEPROM are needed**.

Flash Applications

- Flash applications by density/power/speed requirements:
 - 1M, 2M, 4M in code storage: BIOS (PC & peripherals), boot code, etc.
 - 4M, 8M, 16M in code/data storage: cellular, networking, etc.
 - 32M, 64M and higher in mass data storage: video/audio, SSHD w/ ECC
 - 5V/12V for desk-top, equipment, etc.: where power is not an issue
 - 1.8V, 2.2V, 3V for hand-held & battery-operated devices
 - <1.8V for ultra-low power applications: cellular, PDA, etc.
 - higher speed (≤ 120 ns) for machine-to-machine interface
 - lower speed (> 120 ns) for machine-to-human interface: e.g., voice recording
 - Flash technologies are application specific in nature:
 - NOR, stack-gate (AMD, Intel) for code & data storage in cellular, networking: high speed, high integrity and endurance, medium densities
 - NOR, other structures (Atmel, MX, ISSI, SST) for code storage in BIOS, EPROM replacements: lower density, medium/high speed
 - NAND, stack-gate (Toshiba, Samsung) for data storage in digital camera, flash card, etc.: higher density, lower cost/bit w/ some error correction
 - MLC, various structures (SanDisk, Intel) for mass data storage in digital camera, voice recording, SSHD: lowest speed & cost/bit w/ error correction
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Embedded Flash

- Flash is the most challenging memory technology; embedded flash is even more challenging:
 - Device physics is most complex: more factors and trade-off's
 - More close interactions among device, design and process
 - Embedded flash is base-lined with a logic process in a logic fab!!
Successful flash memory makers use dedicated flash fabs!
 - Embedded Flash requires new paradigm:
 - Different emphases: Robustness, portability, re-usability, etc.
 - New barriers: at $<1.8V$ (low power) and $\leq 0.25\mu m$ (scaling)
 - Room for new ideas and differentiating innovation!!
 - Embedded flash is different from socket memory flash:
 - More value driven: functionality, performance, power, security, etc.
 - More challenges: integration w/ logic baseline; diff. trade-off's
 - TTM: needs quick development (~9 mon.) after logic process !!
Normally memory flash is one whole generation behind
 - Higher cost/bit: larger and more robust cells for TTM, no ECC, etc.
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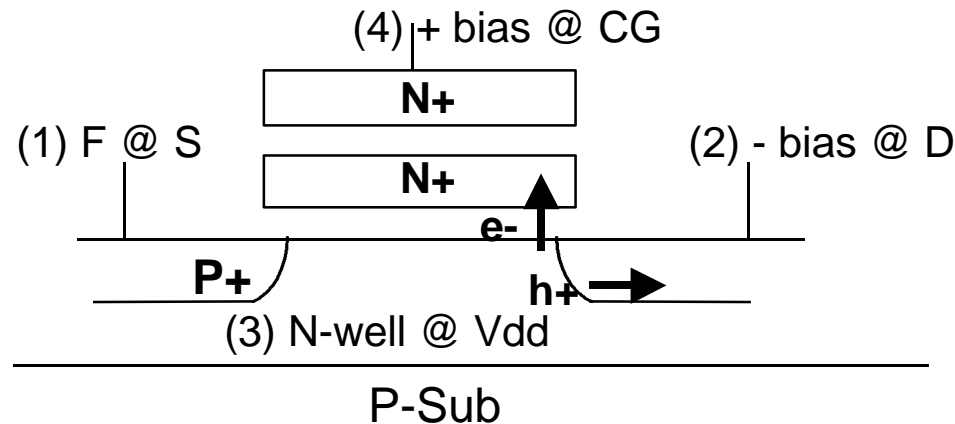
Wish-list for Embedded Flash

- **Compatibility with CMOS Logic:**
 - Embeddable into CMOS Logic process with minimum overhead
 - Little change in logic device characteristics (or SPICE models)
 - Little impact on design libraries (or established design investment)
 - **Low V_{dd}/power operation:**
 - Capable of single-source 1.8V operation and below (down to 0.9V!?)
 - No I_{ds} current (unlike CHE programming) -- small charge pump
 - **Scalable technology & competitive core size:**
 - Lower ownership cost and quicker TTM; lower silicon cost
 - **High endurance and reliability:**
 - No hot hole trapping, localized stress, over-programming & over-erase
 - **Robust and wide (V_{tp}/V_{te}) operating window:**
 - Plug & play; high yield & endurance; quick time-to-market
 - **Simple timing interface:**
 - Deterministic (no complex algorithm); simple circuit designs; easy to use
 - **Granularity:**
 - Flexible density; easy sector partition; unlimited sector size
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Design for an Ideal Embedded Flash

- **Stack-gate structure:**
 - Proven volume manufacturable; self-aligned & scalable
 - Plentiful equipment vendor support (ONO, etcher, etc.)
- **Maintain ~90A to 100A tunnel oxide:**
 - High endurance: >100K cycles
- **About 50/50 divided voltage scheme:**
 - Manage ~14V FN erase voltage req. (in <0.25um CMOS logic)
- **New programming mechanisms needed:**
 - Lower programming current than CHE; faster prog. time than FN
 - Lasting for multiple generations; less process sensitive
 - Page and byte mode programming capabilities
- **FN channel erase:**
 - Uniform field erase w/ sub. at equal potential (no current crowding)
 - No voltage stress on stack-gate side-wall (less process sensitive)
 - Proven for high endurance

Design for an Ideal Flash Cell



Programming (self-regulated by lateral field cancellation):

- | | |
|---|--|
| 1) Float the source | No I_{ds} current (for low power) |
| 2) Bias Drain negative | Remove hot holes from the channel |
| 3) Drain is P-type in N-well
Bias N-well at V_{dd} (or 0V) | BTBT at reverse bias for electron/hole pairs
Repel holes at sub. & stronger bias for BTBT |
| 4) Bias CG positive
Self-regulated programming | Pump electrons up to FG (floating gate)
No current crowding & over-programming |

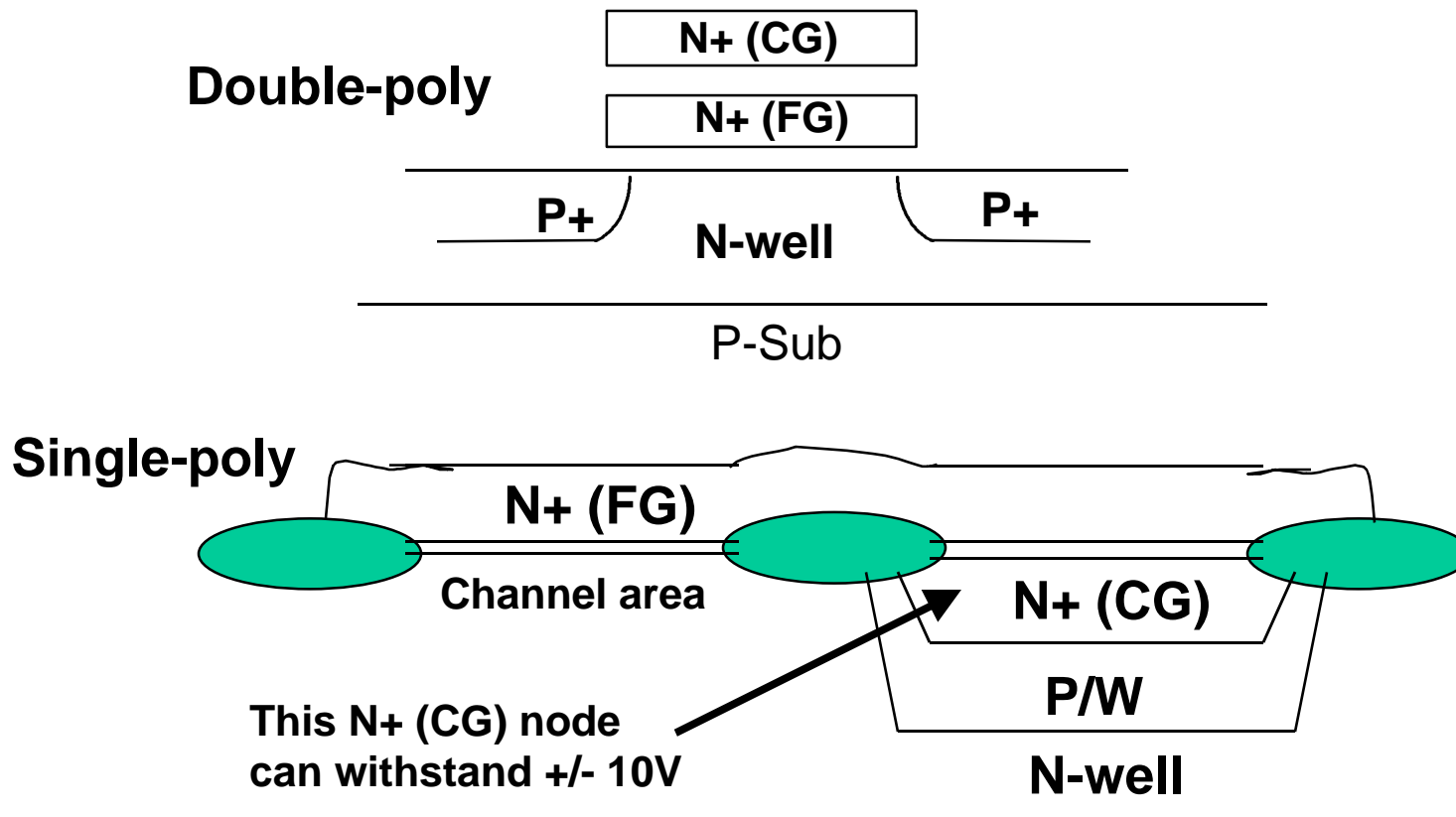
Erase (w/ uniform field to the N-well of the selected sector):

- | | |
|---------------------|-------------------------------------|
| 1) FN channel erase | Avoid side-wall process sensitivity |
|---------------------|-------------------------------------|

Result: P-channel stack-gate with BTBT prog. & FN channel erase!!

Single-poly Embedded Flash

Converting stack-gate into single-poly structure (sharing the same array architecture and circuitry -- design IP reuse):



Key IP for 0.25um Emb. Flash

	Logic Devices	Storage Devices	HV Devices
Desirables:	High performance: same as base-line (B/L) CMOS Logic or Mixed-signal	Robustness, high endurance (>100K to 1M cycles)	Reliable operation
Given:			
Max. operating voltage:	Vdd @ ~2V	~15V (total) for FN erase	~10V (w/ divided volt. Scheme)
Oxide thickness:	Gate oxide @ ~45A	Tunnel oxide @ ~90A -> 100A	Gate oxide @ ~130A
Challenges (STI BV @ ~12V):			
Thermal budget:	Same as B/L	Transparent to logic devices	Transparent to logic devices
Oxide integrity:	As good as B/L	No compromise of high endurance	High integrity

- PMC's key embedded flash patent addresses these issues most cost-effectively
- US Patent # 5,723,355: A method to incorporate NVM and logic components into a single sub-0.3um fabrication process.

SOC Challenges -- Design Aspects

- **0.25um CMOS logic design/product characteristics:**
 - Performance: >200 MHz & higher
 - Data bandwidth (# of I/O): x64 or higher
 - Clock skew & edge rate (di/dt): Tighter and faster
 - **Ground & Vcc bounce noise:** **Much worse (as %)**
 - Vcc range (single P/S): ~2V to 1.8V
 - Interconnect timing budget: ~80% (dominating)
 - RC parasitics & spreading R: Worse (hurt flash Vt control)
 - **Challenges for embedding Flash/E² core:**
 - The on-chip high voltage (routing) must be less than 10V
 - Noise and disturbs are the major problems -- need **isolation**
 - Vt range is narrower for 2V Vdd -- hard to read w/o boosting & pumping
 - A single-transistor cell (with sharing W/L, B/L and S/L) is not robust & manufacturable in all 0.25um SOC environments for “plug-&-play”
 - Vtp and Vte window and distributions are too difficult to control
 - **Solution: 2-transistor cell with select gate is preferred; embedded Flash/E² core in a separated different well**
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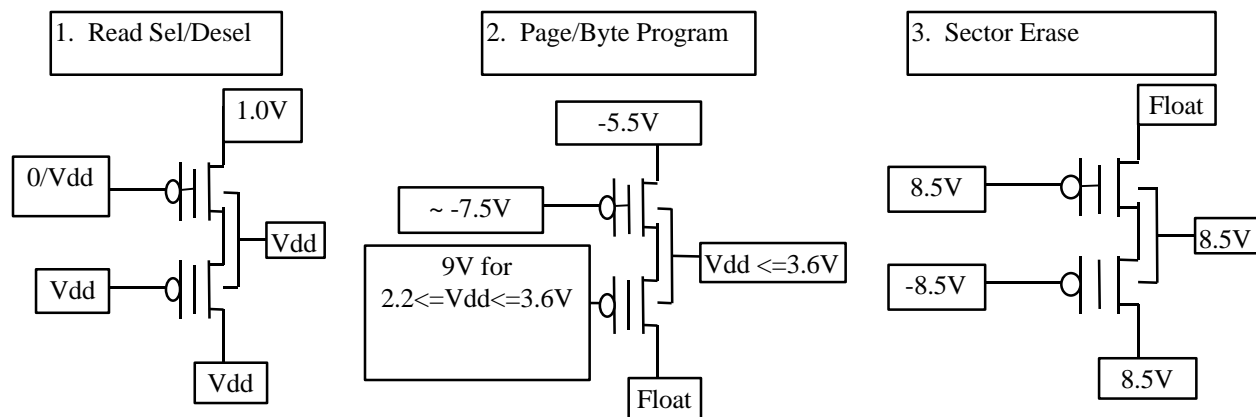
PMC's Embedded ISP NVM Options

- Option 1 with P-EEPROM™ technology
- Options 2 (2-T) & Option 3 (1-T) with P-FLASH™ technology

	Option 1	Option 2	Option 3
Technology	P-EEPROM	P-FLASH	P-FLASH
# of poly	Single	Double	Double
Cell type	EEPROM/NOR Flash	EEPROM/NOR Flash	NOR Flash
# of xtor/cell	2	2	1
Select-gate/cell	Yes	Yes	No
Prog. / Erase states	Deep depl. / Enhan.	Deep depl. / Enhan.	Both enhancement
Cell storage element	Floating gate	Stack-gate	Stack-gate
Flash cell size (um**2)	8 (0.35u), <6 (0.25u)	<2.5 (0.35u), <1.35 (0.25u)	~1.2 (0.35u)
E ² PROM cell size (um**2)	13 (0.35u), 9 (0.25u)	<8 (0.35u), <5.5 (0.25u)	Not applicable
Program mechanism	BTBT	BTBT	CHE
Erase mechanism	FN	FN	FN
Erase window	Yes (>100K cycles)	No (w/ channel erase)	No (w/ channel erase)
Tunnel oxide (A)	~90 at window	100	100
Inter-poly dielectrics	N/A	ONO	ONO
Substrate	P-sub	P-sub	P-sub
Well for cell array	P-well in N-well	N-well	N-well
Operating voltage (LV)	<= 3V	<= 3V	<= 3V
Internal high voltage	~9V	~9V	~9V
# of masking steps	~20	~23	~22

2-T P-Flash Bias Condition

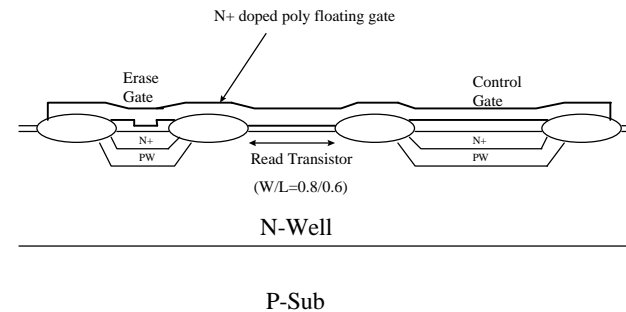
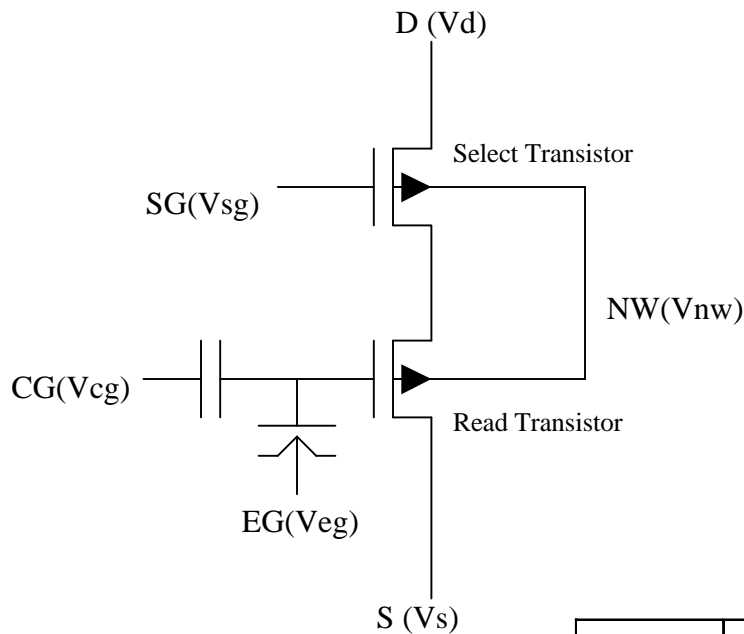
2T Double Poly Flash Cell Read, Program & Erase Operation Modes:



Comments:

- 1) The bias conditions are for a 0.5um Design & Tunnel Oxide Thickness = 100A
- 2) The bias voltages can be scaled down for 0.35um and beyond
- 3) The cell/core size is competitive for high density (>4M) embedded applications

P-EEPROM Bias Condition

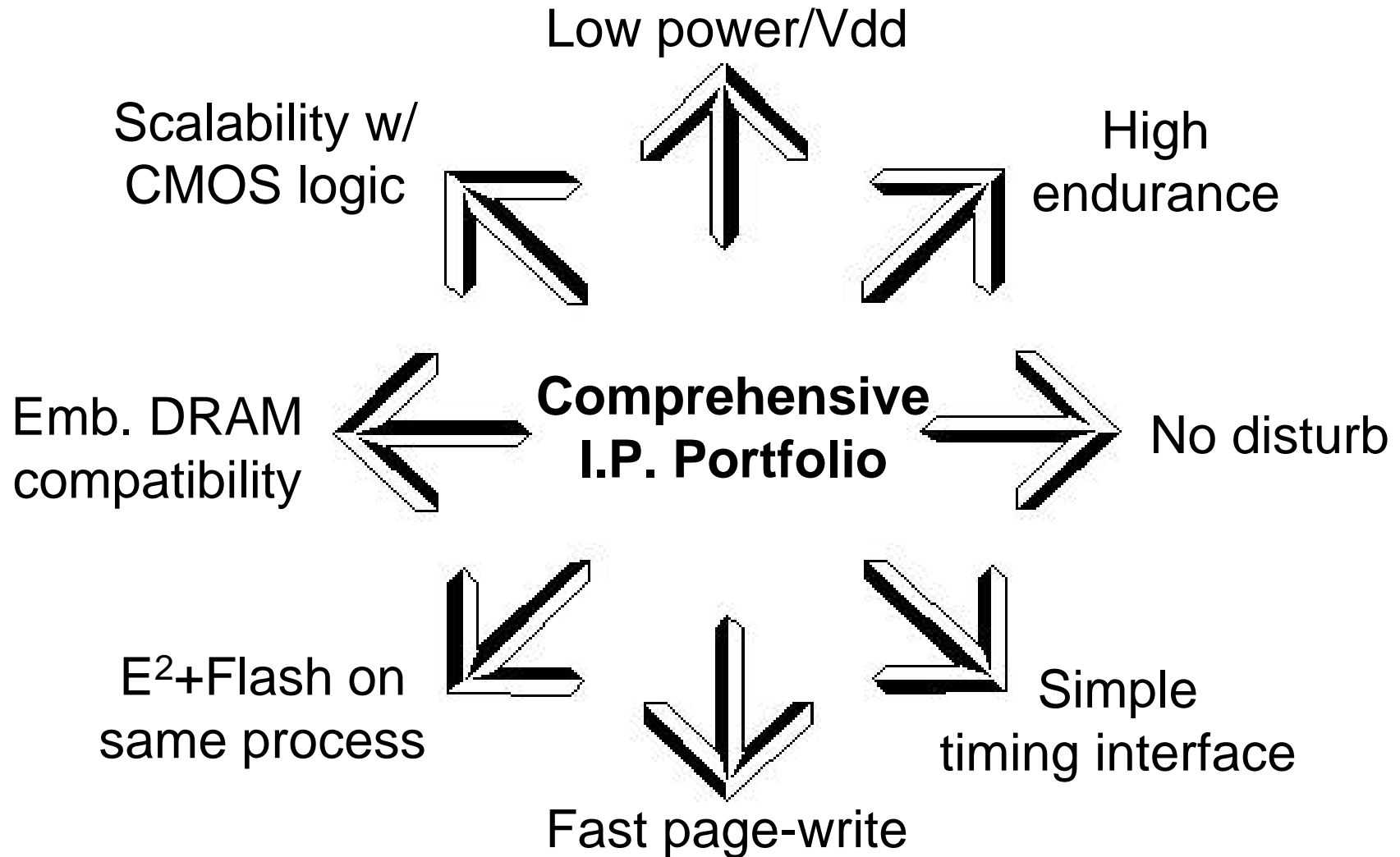


	Vd	Vsg	Vcg	Veg	Vs	Vnw
Prog.	-7	-9	7.5	Float	Float	0
Erase	Float	8.5	-7	7	Float	0
Read	0.7	0.5	Vcc	Float	Vcc	Vcc

Comments:

- 1) This technology is the simplest and robust embedded flash/E² solution
- 2) Ideal for lower density (<=4M) embedded applications

PMC ISP NVM Solution Overview



Key Competitive Advantages

- **Low power and Vdd (@ 3V and below):**
 - Low prog. Volt/current; low erase current; no pumping for read (for 2-T)
- **Scalability w/ CMOS logic (@ 0.25um and below):**
 - Divided/low voltage scheme; scalable cell structure; no special process
- **Embedded DRAM compatibility (especially for single-poly):**
 - Simplest in process integration; no incompatible process steps
- **E²+Flash on same process flow:**
 - Both with 2-T cells; larger cell for E² with larger coupling capacitance
- **Fast page-write (even at low Vdd):**
 - Utilize BTBT fast programming mechanism; low prog. current
- **Simple timing interface (deterministic & no wait-state):**
 - No algorithmic Vt margin control; 2-T for E² type timing; easily portable
- **No disturb (from adjacent-cell operations or Vdd/Gnd bounces):**
 - Robust cell margins (Vtp/Vte @ depl./enh.); 2-T with adequate cell isolation
- **High endurance (and good data retention too w/ thicker tunnel oxide):**
 - No hot-hole trapping; uniform field w/o hot spots; little DC cell currents

Comparison: Device/Tech. Aspects

Cell Type: Mechanism: Vendor Example:	2P/xM (2-T) BTBT/FN PMC	ETOX CHE/FN (N-Ch.)	DINOR FN/FN (N-Ch.)	Split Gate CHE/FN (N-Ch.)
Sensitivity to Disturbs with scaling	Low	High	High	High (CG & SG tied together)
Sensitivity to Over-Program or Over-erase	None	High	High	None
Cell Current During Write	< 10nA	100's μ A	< 1nA	< 1 μ A??
Process Complexity	Medium	Medium	High (3P/2M or 2P/3M)	High (non-self aligned process)
Cell Process Alignm't Sensitivity	Low	Low	Low	High (non-self-aligned process)
Hot Hole/Interface Damage During Write (intrinsic limit to endurance)	No	Yes	Yes	No (but inter-poly oxide scalability limits endurance)
Ease of Process Integration with Logic	Easiest	Medium (but non-symmetry junctions)	Difficult	Difficult
Compatibility with 0.25 μ logic process	Yes	No	No	No

Comparison: Design/Product Aspects

Cell Type: Mechanism: Vendor Example:	2P/xM (2-T) BTBT/FN PMC	ETOX CHE/FN (N-Ch.)	DINOR FN/FN (N-Ch.)	Split Gate CHE/FN (N-Ch.)
Vtp/Vte Operation margin @ 2V	Very Wide	Narrow	Narrow	Can be sensitive to cycling
Disturb Concerns	None	Severe	Severe	Less
Needs Embedded Write Algorithm?	No	Yes	Yes	No
Page Mode?/Size Page Prog Time	Yes/256Bytes 100µs/page	No	Yes/256Bytes 15ms/page (1)	Yes/256Bytes 5ms/page (2)
Byte Mode Prog? Byte Prog Time	Yes 10µs	Yes 10µs	No	Yes 30µs (2)
Mixed EEPROM/Flash?	Yes	No	No	No
Time To Market	<u>Fast:</u> (Less process/design sensitive)	<u>Slow:</u> (Cell cannot overerase: sensitive to process/design)	<u>Slow:</u> (Cell cannot overprogram: sensitive to process/design)	<u>Slow:</u> (Non-standard process → yield/reliability concerns)
Notes			(1) Mitsubishi 8Mb	(2) No page & byte modes in same part

Status Update

- Demonstrated both 1-P & 2-P, 2-T technologies at 0.5um at TSMC:
 - 1-P with outstanding product characteristics and reliability is in final qual and pilot production (silicon data to be published soon)
 - 2-P with working silicon is in optimization stage
- 0.35um development in progress at another foundry
- Working with technology partners/licensees in both technologies at 0.35um and beyond
- PMC is promoting these 2 embedded flash technologies to be a de-facto standard for 0.25um SOC:
 - Building strategic partnership with licensees
 - Teaming up w/ EDA vendors for tool supports (design IP re-use)
 - Teaming up w/ design service partners to support licensees
 - Working with foundry partners to support fab-less licensees
 - Building strategic partnership with ASIC houses/licensees to provide system end users one-stop service

Summary

- **Comprehensive I.P. protection:**
 - 19 granted US patents & 7 granted overseas, and more pending
 - Over 30 US patents cover key mainstream & emerging products
 - NOR, NAND, MLC and embedded NVM solutions
 - **Scalable & robust NVM technologies:**
 - Disturb-free and robust solutions for quick TTM
 - Same process for stand-alone and embedded applications
 - Require mainstream process modules, no special effort
 - Scalable to 0.18um and beyond; easier portable
 - **Product capability differentiation:**
 - Low voltage/power: Easier implementation for 1.8V and lower
 - Faster programming capability at lower Vcc
 - Easier integrating Flash & full-feature E² in the same process
 - **World-class partnership:**
 - Established top-tier license partnership on $\leq 0.25\mu\text{m}$
 - Key endorsements for both embedded Flash & EEPROM
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Technologies for Licensing

PMC offers **comprehensive IP** portfolio to its licensees:

- For state-of-the-art **embedded Flash/EEPROM applications**:
 - **1P/xM, 2-T, P-channel Flash/EEPROM technology**:
 - Ideal for medium density (< 4M) embedded Flash/EEPROM core
 - Most logic-like process (keep same device models & logic design library)
 - Most compatible with embedded DRAM core
 - Highly manufacturable and scalable; Robust and disturb-free; Valued-added features
 - **2P/xM, 2-T, P-channel Flash/EEPROM technology**:
 - Ideal for high density (>4M to 16M) embedded Flash/EEPROM core
 - Highly manufacturable and scalable; robust and disturb-free; valued-added features
- For high-density Flash memory products:
 - 2P2M, 1-T, P-channel **NOR Flash** (US Pat. #5,687,118)
 - P-channel **Multi-Level Cell Flash** (US Pat. # 5,666,307)
 - P-channel **NAND Flash** (US Pat. # 5,581,504)